Page 2, line 24+:

Disclosed herein is a family of emitter controlled thyristors (ECT) and emitter turn-off thyristors ETO employing a plurality of control schemes for turning the thyristor on and off. In a first embodiment of the present invention a family of thyristors are disclosed all of which comprise a pair of MOS transistors, the first of which is connected in series with the thyristor (hence after called emitter switch, or Q_E or Q1) and a second which provides a connection from the thyristor gate to the cathode or ground (hence after called gate switch or Q_G or Q2). A third optional MOSFET (hence after called Q_{ON} or Q3) is used to provide the turn-on mechanism for the thyristor. Depending on whether a n-channel or p-channel device is used for Q_E. A negative voltage applied to the gate of the first MOS causes the thyristor to turn on to conduct high currents. A zero to positive voltage applied to the first MOS gate causes the thyristor to turn off. A negative feedback mechanism also exist between the Q_E and Q_G at high currents that causes the ECT to operate at its breakover boundaries of the latching condition with the NPN transistor portion of the thyristor operating in the active region. Under this condition, the anode voltage V_A continues to increase without significant anode current increase. ETO devices disclosed here also use at least two switches Q_G and Q_E to control the current. They also have the negative feedback mechanism that causes the current to saturate at high currents. In particular, ETO fabrication packages are also disclosed having packaged semiconductor devices controlling the thyristor.

Page 6, line 31+:

The ECT can be turned-off by increasing the gate electrode voltage to zero or positive value in PMOS1

10, which interrupts the main current flow path. All currents are then forced to divert to the cathode by the PMOS2 20. Both emitter switch (PMOS1) and emitter short (PMOS2) are used in the turn-off of the ETC., and unlike in the EST, no parasitic thyristor limits the reverse bias safe operation area (RBSOA) of the ECT.

Page 15, line 13+:

Referring now to Figures 7A-B, there is shown a cross-sectional view of the Single Gate NMOS ECT (SNECT) and its equivalent circuit, respectively. The SNECT has a 4-layer PNPN thyristor structure 2 in series with a N channel MOSFET (NMOS 1) 150 integrated on the top of the P well through a Floating Ohmic Contact (FOC) metal strap 152. The FOC 152 connects the upper N+ emitter 154 of the PNPN thyristor and the N + drain region 156 of the NMOS 1. An N-channel depletion mode MOSFET (NMOS2) 162 is also integrated at the surface of the SNECT which acts as the turn-on MOSFET. A P-channel MOSFET (PMOS) 160 is formed between two P regions. The NMOS2 162 and the PMOS 160 share the same gate 164, and the gate is directly tied to the cathode contact 166; hence, the SNECT is a three-terminal device.

Page 16, line 23+:

Referring now to Figures 8A-B, there is shown a cross-sectional view of a single gate emitter controlled thyristor SECT and its circuit equivalent, respectively. The SECT has a 4-layer PNPN thyristor structure 2 in series with a P channel MOSFET (PMOS1) 180 integrated on the surface of the N substrate through a Floating Ohmic Contact (FOC) metal strap 182. The FOC 182 connects the upper N+ emitter 184 of the PNPN thyristor and the P source region 186 of the PMOS1 180. The FOC 182 provides the bridge for transferring emitter electron currents of the upper NPN transistor